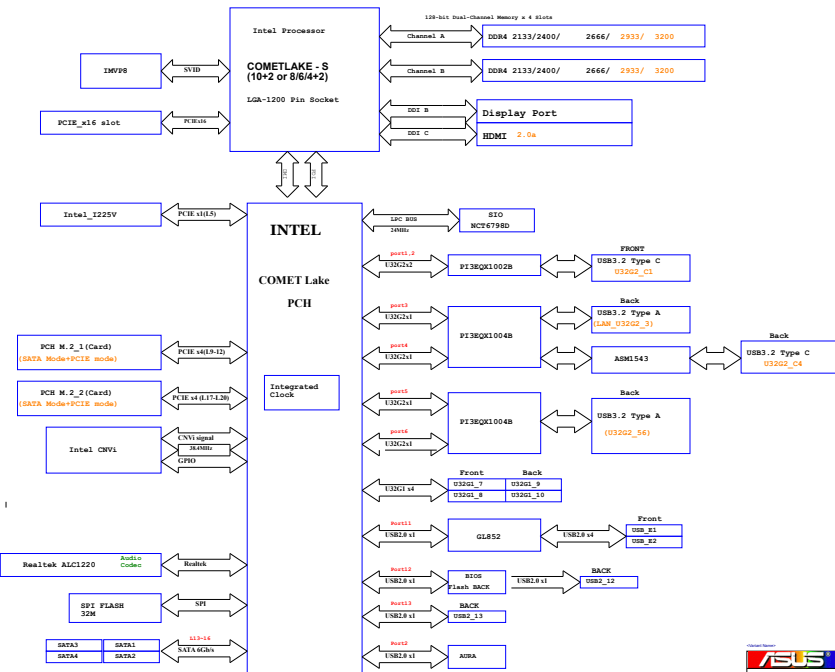
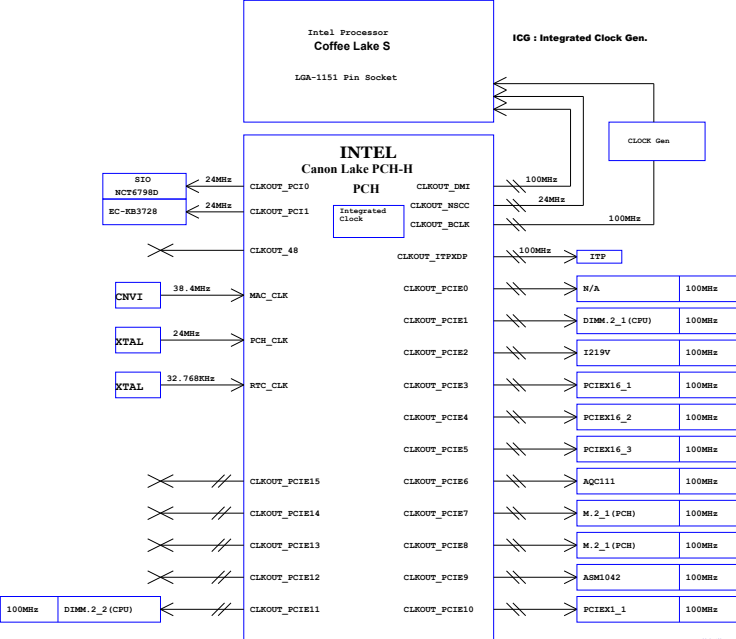


2019.11

## Z490-I



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-Reserved Name-












<Variant Name>

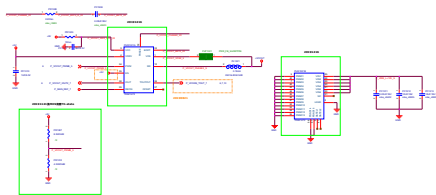
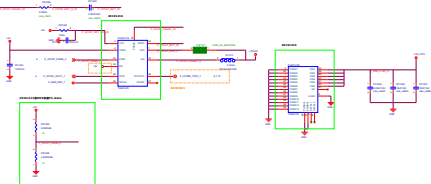
		<b>Title :</b> <b>VCORE DRIVER2</b>	
<b>ASUSTek COMPUTER INC.</b>		<b>Engineer:</b> <b>Mandy</b>	
Size	Project Name		Rev
A1	<b>COMET LAKE</b>		R1.00
Date:      Thursday, December 12, 2019		Sheet      8      of      121	

<Variant Name>

	<b>Title :</b> empty
---	----------------------

ASUSTeK Computer Inc.	<b>Engineer:</b>
-----------------------	------------------

Size	Project Name	Rev
A	<b>Maximus XI Extreme</b>	R1.01



PCB layout for a Maxim 89000 microcontroller. The layout includes a green box for the microcontroller, an orange box for the crystal, and a blue box for the pull-up network. The microcontroller is connected to a crystal and a pull-up network. The pull-up network is connected to a 5V supply. The crystal is connected to the microcontroller's crystal pins. The pull-up network is connected to the microcontroller's I/O pins. The layout is shown in a top-down view.





**Title :** empty

ASUSTeK Computer Inc.

**Engineer:**

Size

Project Name

Rev

A

**Maximus XI Extreme**

R1.01







<Variant Name>



**Title :** empty

ASUSTeK Computer Inc.

**Engineer:**

Size

Project Name

Rev

A2

**Maximus XI Extreme**

R1.01

Date: Thursday, December 12, 2019

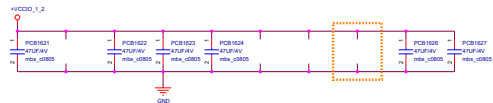
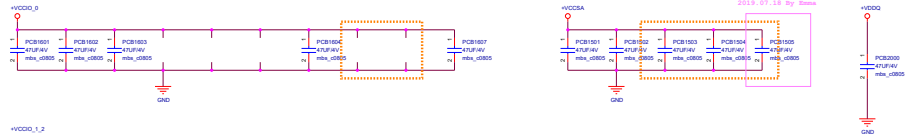
Sheet 14 of 152

<Variant Name>

	<b>Title :</b> empty
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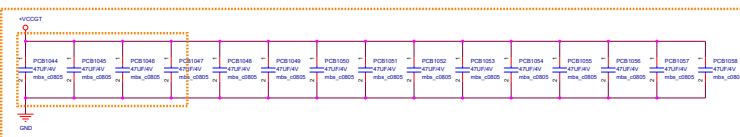
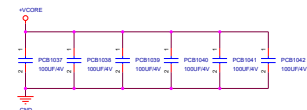
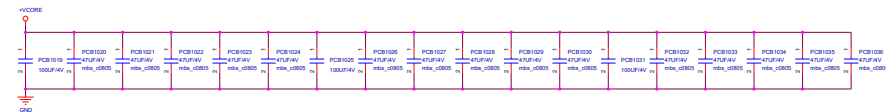
ASUSTeK Computer Inc.	<b>Engineer:</b>
-----------------------	------------------

Size	Project Name	Rev
A	<b>Maximus XI Extreme</b>	R1.01



20190702

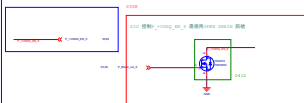
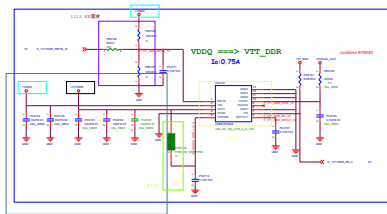
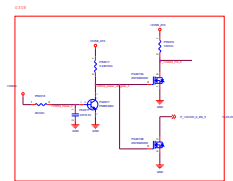
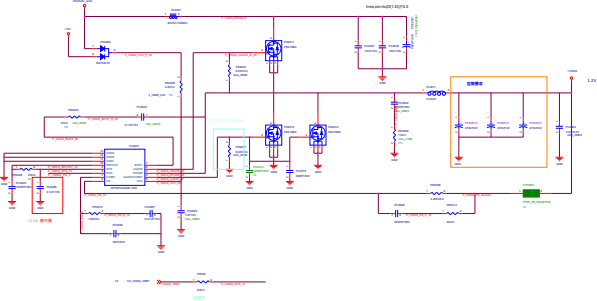
www.teknisi-indonesia.com



20190702 for GT, TOP\*4, BOT\*7

<Insert Name>

<b>ASUS</b>		<b>Title :</b>	VCCORE MLC&CAP
ASUS& Computer Inc.		<b>Engineer:</b>	Miles Liu
Size	Project Name		
Custom	Maximus XI Extreme		
Date	Tuesday, December 11, 2019	Sheet	16 of 165



0205

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**Title :**

ASUSTek COMPUTER INC.

**Engineer:**

Size

Project Name

Rev

A3

R1.01

Mode pin	Light Load Value	Switching Frequency
VCC	Pulse Skip	600KHz
24kΩ to GND	Pulse Skip	800KHz
121kΩ to GND	Pulse Skip	1000KHz
GND	Forced CCM	600KHz
30.1kΩ to GND	Forced CCM	800KHz
60.4kΩ to GND	Forced CCM	1000KHz

lin = 2.965A

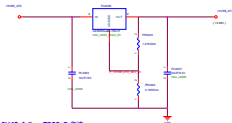
CAUTION: Mode pin should be placed close to SWIFT (SW) Mode, Skip, and Stand-by pins to short pin(s).

20191018

teknisi indonesia

1.8V\_A上通路

# +5VSB\_ATX 與 +3VSB\_ATX



+3VSB follow Z390-I 作法

# +5VSB與+5VDUAL\_AUX合併



空間需求移除+1.8V\_A, SR959需上件

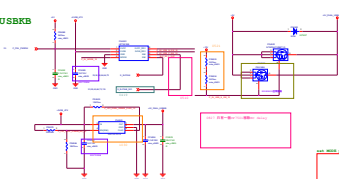
# +3VSB\_ATX --> +3VSB SEQUENCY



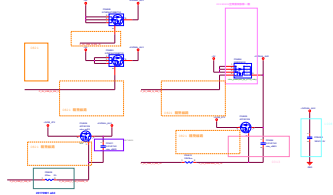
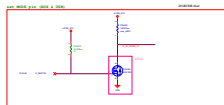
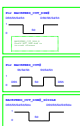
2019GB11合併到+1.8V\_A

Document



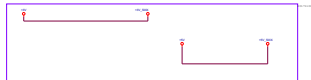
**USBKE**

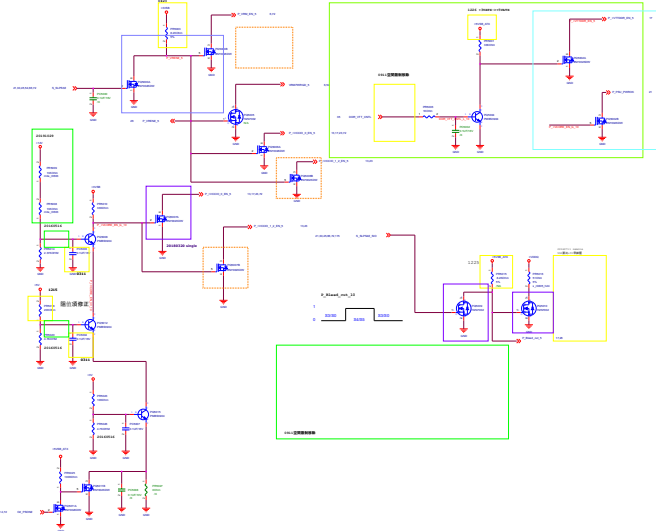
5VDUAL\_AUX



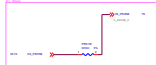



透過AUDIO開關





2025/05/06 10:00:00 100% 100%



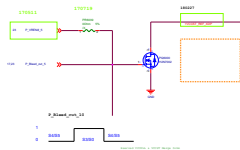
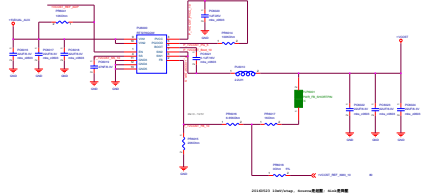
20160520 follow Note Z170

2016.01.07

2016.07.24  
follow Z160 結~終  
w/ Kana

\*Client Name

		Title : +SVSB_AUD	
ASUS COMPUTER INC.		Engineer: RAY	
Name	Project Name		Date
Custom	Maximus XI Extreme		01/01
Date: 2016/01/01 Version: 1.0 2016			



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www.pearsoned.com.cn



**Title :** CPTH (CNVi)

ASUSTek Computer Inc.

**Engineer:** Aaron\_Su

Size

A4

Project Name

**Maximus XI Extreme**

Rev

R1.01

Date: Thursday, December 12, 2019

Sheet 27 of 152



**Title :** CPTH (CNVi)

ASUSTek Computer Inc.

**Engineer:** Aaron\_Su

Size

Custom

Project Name

**Maximus XI Extreme**

Rev

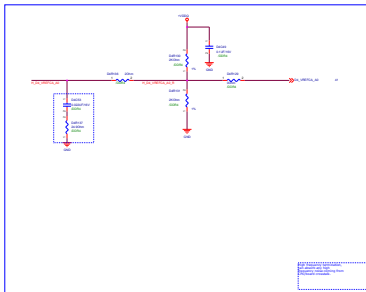
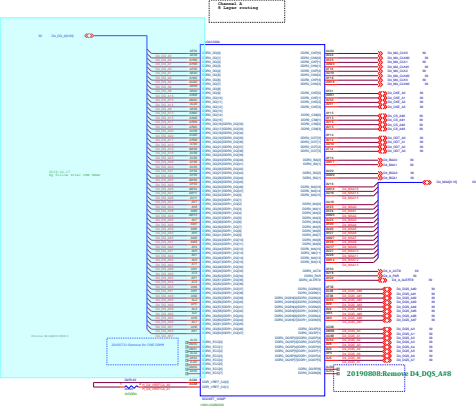
R1.01

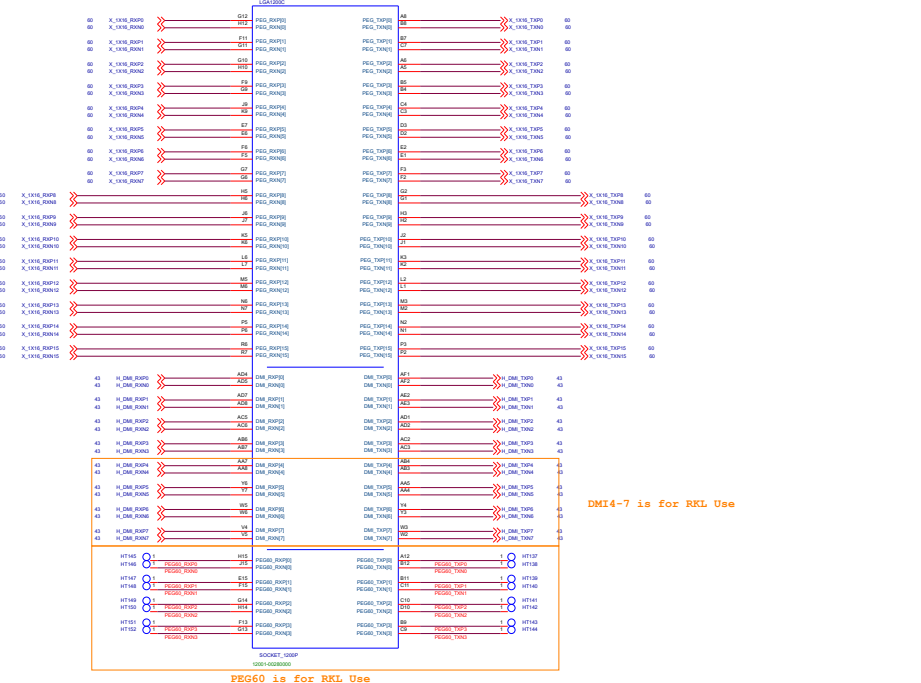
Date: Thursday, December 12, 2019

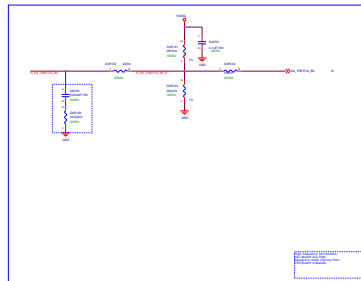
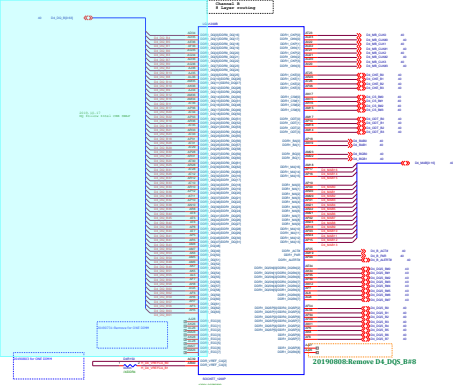
Sheet 28 of 152











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+VDDQ Power Monitor

+VCCGT Power Monitor

+5V Power Monitor

+VCCSA Power Monitor

+VCCORE Power Monitor

+1.05V\_A Power Monitor

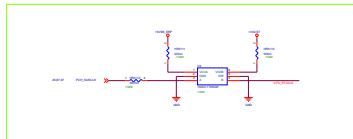
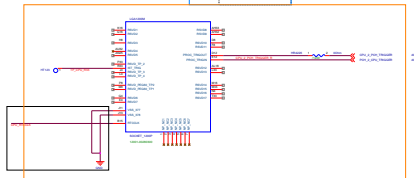
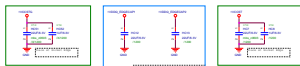
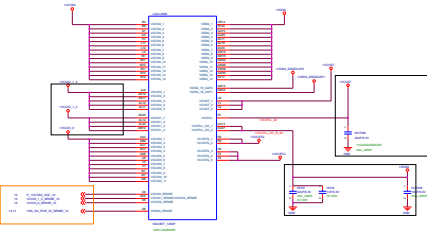
+VCCIO Power Monitor

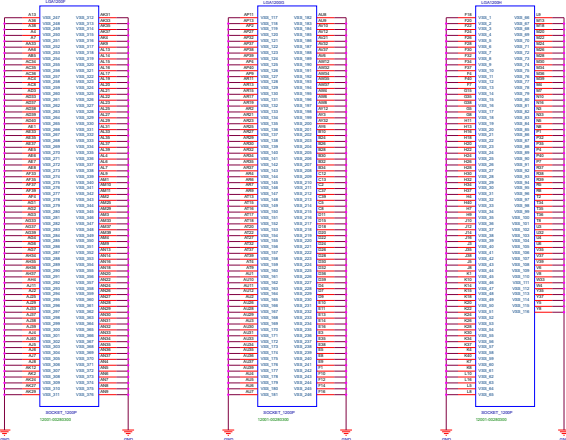
+5VSB\_ATX Power Monitor

+3VSB\_ATX Power Monitor

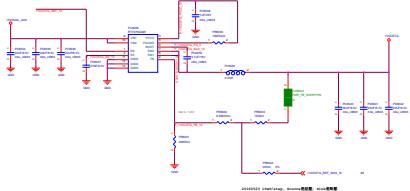
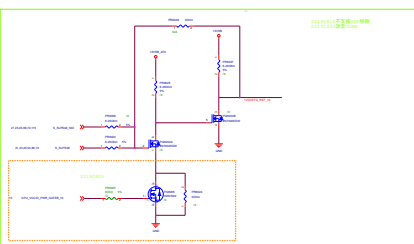
A1	A2	Address
Grnd	Grnd	1000000 : 40
Grnd	Vcc	1000000 : 41
Grnd	SDA	1000100 : 42
Grnd	SCL	1000101 : 43
Vcc	Grnd	1000100 : 44
Vcc	Vcc	1000101 : 45
Vcc	SDA	1000110 : 46
Vcc	SCL	1000111 : 47
SDA	Grnd	1001000 : 48
SDA	Vcc	1001001 : 49
SDA	SDA	1001010 : 4A
SDA	SCL	1001011 : 4B
SCL	Grnd	1001100 : 4C
SCL	Vcc	1001101 : 4D
SCL	SDA	1001110 : 4E
SCL	SCL	1001111 : 4F

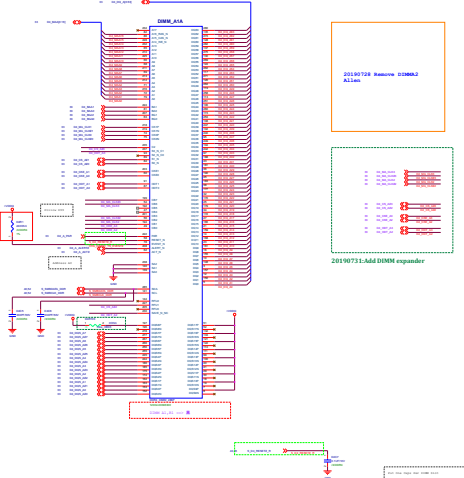
ASUS



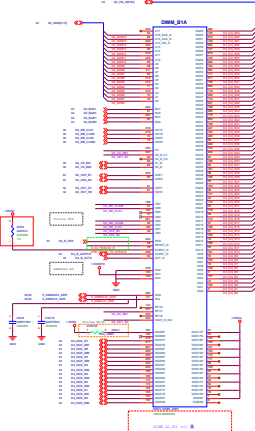


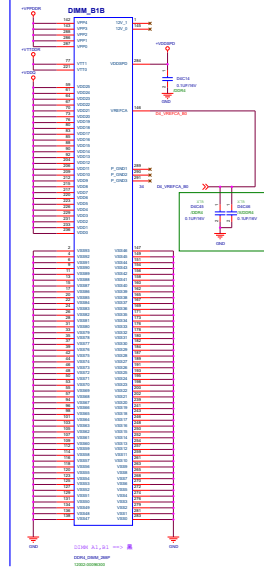
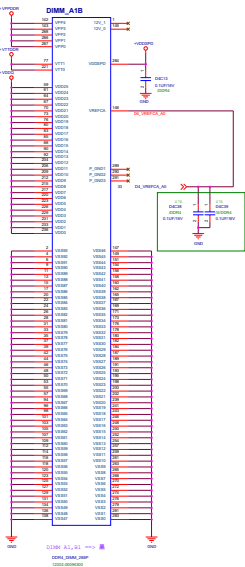






teknisi indonesia



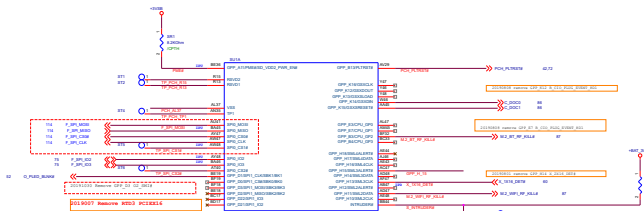


預留VDDSPD Fuse, DOA/FA改善Solution.

非ROG機請自行改小顆Fuse.

Copyright Notice

Remove 20K LED



```

MPC Flash sharing mode
0-Master ATTACHED FLASH SHARING
1-Slave ATTACHED FLASH SHARING
PCN HAS INTERNAL WRK DO

```



2022-2023  
Year 2022

20240404\_Rumours Yellow.indd 2

CONSENT STRIP IS ENABLE IF LOW  
SOLAR HAS INTERLOCK, WHILE PU  
See External Flash Postcard.



Page 10/10

20190404\_Ramona\_Rollney\_0490C

STABILITY STRAP IS ENABLED IF LOW  
FOR HAS INTERVAL BEEN 90



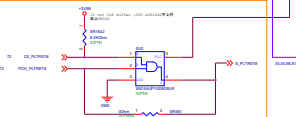
```

#SPI Flash Sharing Mode
# = Master Attached Flash Sharing (#SPI) enabled (default)
# = Slave Attached Flash Sharing (#HLS) enabled
Notes:
# 1. the internal pull-down is disabled after B080016 de-asserts.
# 2. this signal is in the primary mode.
# Warning: this string must be configured to '0'
# (#HLS is disabled) if the #SPI or L2C strap is configured to '0' (#SPI is disabled)

```

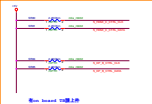
JMFC.GOV IS OBTAINED IF LOW  
FOLLOW SUPPL.O.

Reserved  
 External pull-up is required. Maximum I/OH if pulled up to 3.3V or 5V if pulled up to 3.3V.  
 This strap should sample HIGH. There should NOT be any on-board device driving in the opposite direction during strap sampling.









PS\_ONB Control via CEC

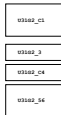


PS\_ONB

Back

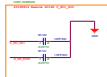
Back

Back



PS\_ONB

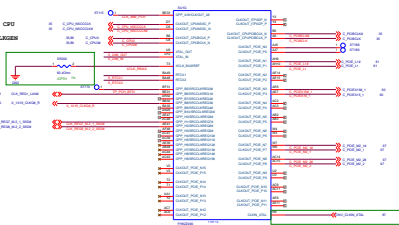
PS\_ONB\_DETECT change to ESD





For CPU  
To CLEMEN

10 0.0V  
10 1.0V  
10 0.0V  
10 1.0V  
10 0.0V  
10 1.0V  
10 0.0V  
10 1.0V



For XDP

For CPU

Intel LAN I225V

PCINX1\_1

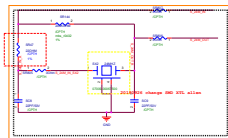
For PCIe Slot X16\_1

For PCIe Slot X16 2

For M.2 1

For M.2 2

Follow CRB



20190807 Remove RTD3  
20190731 Allen Remove

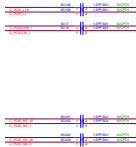
20190731 Allen Remove

For RTD3 use

20190731 Allen Remove

For RTD3

page 100mka



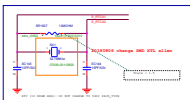
xxxiv 1. October

to CPU 100ms

PCIe ref CLK to CPU 100MHz

CLK from Crystal to CPU 24MHz

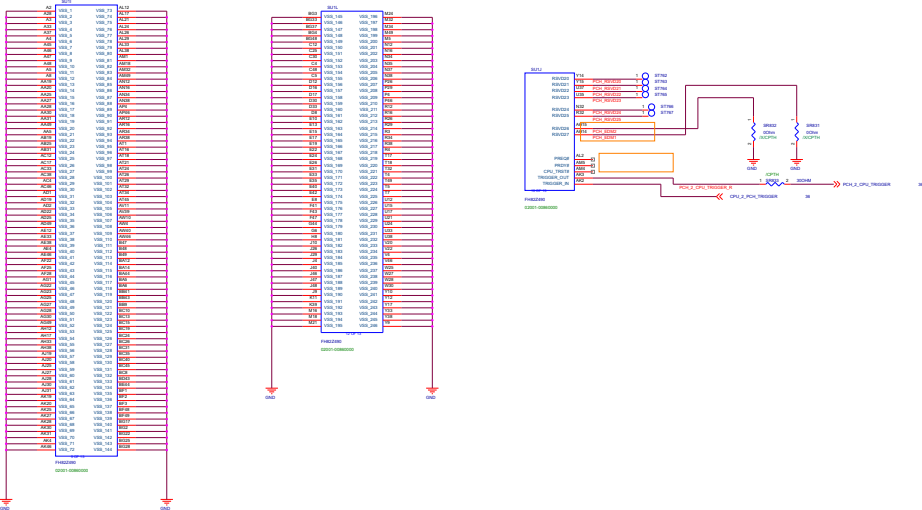
	0.4s	0.5s
0 CPU BUSIO	0	0

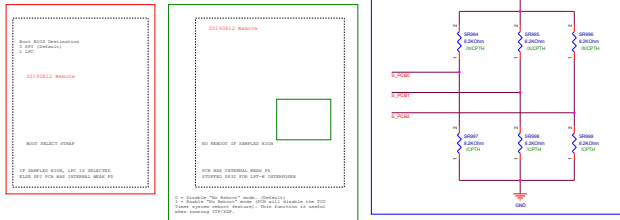
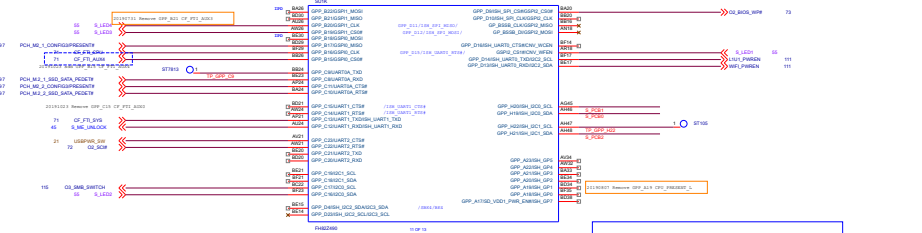


For SD ESD Protection









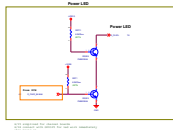
```
if use CMM => SR760 remove/ SR313 stuff
if don't use CMM => SR760 stuff
```



GDP\_26 Group

DOI: 10.1002/for

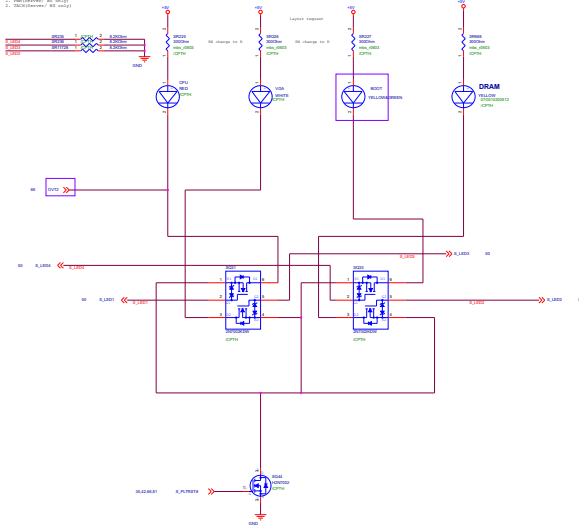












Layout for D03



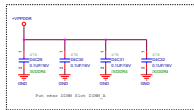
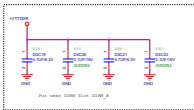
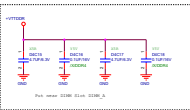
20190812 Resonance Run 20386



20190812 Resonance Run 20386



20190812 Resonance Run 20386



©Maxim Design



<Signal Name>

		Title : DDR4 (SMBUS/SPD)	
ASUSTeK Computer Inc.		Engineer: Eason	
Item	Project Name	File	
A3	Maximus XI Extreme	R1.01	
Date: Thursday, September 12, 2019			
Drawn	By	Chk	App



**Title :** CPTH (CNVi)

ASUSTek Computer Inc.

**Engineer:** Aaron\_Su

Size

A1

Project Name

**Maximus XI Extreme**

Rev

R1.01

Date: Thursday, December 12, 2019

Sheet 58 of 152

For add-in card only in X16\_1 & X16\_2

ALL CFG 1 = NO VERIFICATION ON BOARD DEFAULTS HIGH  
ALL CFG 2 = VERIFICATION STRAP LOW ON BOARD

Configuration Strap Table Rev 1.0

All Strap Settings Table Rev 1.0			
CFG	Strap	Strap	Strap
1	Strap	Strap	Strap
2	Strap	Strap	Strap
3	Strap	Strap	Strap
4	Strap	Strap	Strap
5	Strap	Strap	Strap
6	Strap	Strap	Strap
7	Strap	Strap	Strap
8	Strap	Strap	Strap
9	Strap	Strap	Strap
10	Strap	Strap	Strap
11	Strap	Strap	Strap
12	Strap	Strap	Strap
13	Strap	Strap	Strap
14	Strap	Strap	Strap
15	Strap	Strap	Strap
16	Strap	Strap	Strap
17	Strap	Strap	Strap
18	Strap	Strap	Strap
19	Strap	Strap	Strap
20	Strap	Strap	Strap
21	Strap	Strap	Strap
22	Strap	Strap	Strap
23	Strap	Strap	Strap
24	Strap	Strap	Strap
25	Strap	Strap	Strap
26	Strap	Strap	Strap
27	Strap	Strap	Strap
28	Strap	Strap	Strap
29	Strap	Strap	Strap
30	Strap	Strap	Strap
31	Strap	Strap	Strap
32	Strap	Strap	Strap
33	Strap	Strap	Strap
34	Strap	Strap	Strap
35	Strap	Strap	Strap
36	Strap	Strap	Strap
37	Strap	Strap	Strap
38	Strap	Strap	Strap
39	Strap	Strap	Strap
40	Strap	Strap	Strap
41	Strap	Strap	Strap
42	Strap	Strap	Strap
43	Strap	Strap	Strap
44	Strap	Strap	Strap
45	Strap	Strap	Strap
46	Strap	Strap	Strap
47	Strap	Strap	Strap
48	Strap	Strap	Strap
49	Strap	Strap	Strap
50	Strap	Strap	Strap
51	Strap	Strap	Strap
52	Strap	Strap	Strap
53	Strap	Strap	Strap
54	Strap	Strap	Strap
55	Strap	Strap	Strap
56	Strap	Strap	Strap
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69	Strap	Strap	Strap
70	Strap	Strap	Strap
71	Strap	Strap	Strap
72	Strap	Strap	Strap
73	Strap	Strap	Strap
74	Strap	Strap	Strap
75	Strap	Strap	Strap
76	Strap	Strap	Strap
77	Strap	Strap	Strap
78	Strap	Strap	Strap
79	Strap	Strap	Strap
80	Strap	Strap	Strap
81	Strap	Strap	Strap
82	Strap	Strap	Strap
83	Strap	Strap	Strap
84	Strap	Strap	Strap
85	Strap	Strap	Strap
86	Strap	Strap	Strap
87	Strap	Strap	Strap
88	Strap	Strap	Strap
89	Strap	Strap	Strap
90	Strap	Strap	Strap
91	Strap	Strap	Strap
92	Strap	Strap	Strap
93	Strap	Strap	Strap
94	Strap	Strap	Strap
95	Strap	Strap	Strap
96	Strap	Strap	Strap
97	Strap	Strap	Strap
98	Strap	Strap	Strap
99	Strap	Strap	Strap
100	Strap	Strap	Strap

# CFG[6:5]: PCI Express\* Bifurcation

- 00 = 1 x8, 2 x4 PCI Express\*
- 01 = reserved
- 10 = 2 x8 PCI Express\*
- 11 = 1 x16 PCI Express\*

©2010 ASUS

<b>ASUS</b>		Title : QUICK SWTPCPCXH.1	
ASUS COMPUTER INC.		Engineer: Aaron_Su	
Rev	Original Name	Rev	1.01
A3		Maximus XI Extreme	
Date	Thursday, December 10, 2010	Drawn	00 02 10



**Title :** CPTH (CNVi)

ASUSTek Computer Inc.

**Engineer:** Aaron\_Su

Size

A1

Project Name

**Maximus XI Extreme**

Rev

R1.01

Date: Thursday, December 12, 2019

Sheet 61 of 152

陳永堯 Dr. Yau-Luen Chan 809210

		Title : CP004/CNVQ	
Effective Date/Version:		Engineer: Aaron_Su	
Rev	Engineer's Name	Maximus XI Extreme	Rev
02			02
Created: Engineer's ID: 0000		Date: 02/02/2014	

Main Link Clocking need 50 100K

T3 modify ok

50K request - 40K 50 1K - 50 100K (overstiff)  
50K request - 40K 50 1K - 50 100K (overstiff)  
50K - 40K 50 1K - 50 100K (overstiff)  
50K - 40K 50 1K - 50 100K (overstiff)

T3 modify ok

Choke 改回300 nH (原本約)  
2018/01/30 Bowerl

Parade 2017/11/22 Bowerl

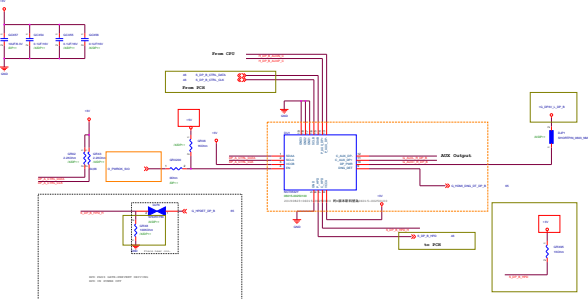
Parade 2017/11/22 Bowerl

改GP5料 2017/12/28 Bowerl

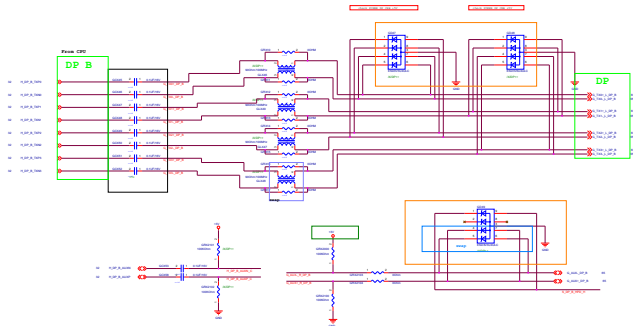
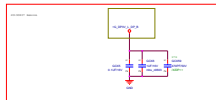
qqcc 修改kcm 2017/12/20 Bowerl

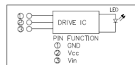
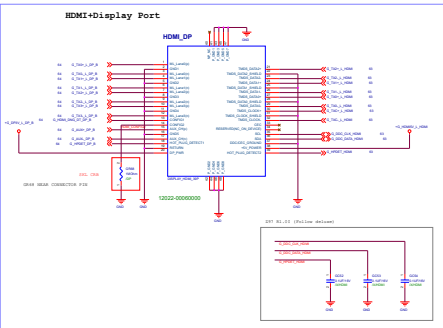
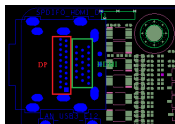
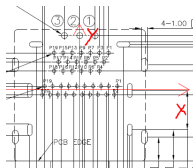
ASUS





Layout Guide:  
 1.) Place the input capacitor(s) near the VCCIN pin as close as possible.  
 2.) Output decoupling capacitor(s) have to be placed near the load as close as possible for decoupling high frequency signals.  
 3.) Keep VCCIN and DP pins traces wide and short.  
 4.) The GND should be connected to a strong ground plane for heat sink





## 7. HDMI AND DP PIN ASSIGNMENTS:

HDMI			
PIN NO.	SIGNAL ASSIGNMENT	PIN NO.	SIGNAL ASSIGNMENT
P1	TMDS DATA+	P2	TMDS DATA+ SHIELD
P3	TMDS DATA-	P4	TMDS DATA+
P5	TMDS DATA SHIELD	P6	TMDS DATA-
P7	TMDS DATA+	P8	TMDS DATA+ SHIELD
P9	TMDS DATA-	P10	TMDS CLOCK+
P11	TMDS CLOCK SHIELD	P12	TMDS CLOCK-
P13	CEC	P14	RESERVED (SW-DR-DEVICE)
P15	SCL	P16	SDA
P17	EDC/CEC GROUND	P18	+5V POWER
P19	HOT PLUG DETECT		

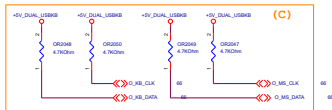
  

DISPLAYPORT			
PIN NUMBER	SOURCE-SIDE PIN ASSIGNMENT	SINK-SIDE PIN ASSIGNMENT	
P1	M_Lane B(p)	M_Lane 3(p)	
P2	GND	GND	
P3	M_Lane B(n)	M_Lane 3(p)	
P4	M_Lane G(p)	M_Lane 2(n)	
P5	GND	GND	
P6	M_Lane G(n)	M_Lane 2(p)	
P7	M_Lane B(p)	M_Lane 3(n)	
P8	GND	GND	
P9	M_Lane G(n)	M_Lane 2(p)	
P10	M_Lane B(p)	M_Lane 3(n)	
P11	GND	GND	
P12	M_Lane 3(n)	M_Lane B(p)	
P13	CONF IG	CONF IG	
P14	CONF IG	CONF IG	
P15	AUX CH G(p)	AUX CH G(p)	
P16	GND	GND	
P17	AUX CH G(n)	AUX CH G(n)	
P18	HOT PLUG DETECT	HOT PLUG DETECT	
P19	RETURN	RETURN	
P20	DP PWR	DP PWR	

Document Name:

擇1. By Project 需求:

1. 如無Onboard KBMS connector, 請保留 (C) 框, 刪除 (A) (B) 框.
2. 如connector只有一個KBMS孔, 請留 (A) 框, 刪除 (B) (C) 框.
3. 如connector分別各有一個KB, 一個MOS孔, 請留 (A) (B) 框, 刪除 (C) 框.



<Variant Name>

<b>ASUS</b>		Title : NCT6796D_BF-2	
ASUSTek COMPUTER INC.		Engineer: Eagle	
Size	Project Name		Rev
A3	Standard Circuit		R1.01
Date	Thursday, December 12, 2019	Sheet	67 of 103



## RING Function

remove RING Wake

## COM Box Header

remove COM port header

\*Default Name:

<b>ASUS</b>		Title : NCT6796D_BF-3	
ASUSTeK COMPUTER INC.		Engineer: Aaron_Su	
Model	Project Name	Rev	Rev
A3	Maximus XI Extreme	1.0	1.0
Date: Thursday, December 10, 2020		Printed	68 of 100

## MemOK II Circuit



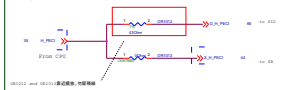
20180112

6/12 revised the circuits to two 0 ohm style

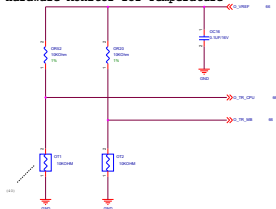
SKL PDG CRB CPU PECI to EC PECI have 43 ohm

Z97 CR1012 0 ohm

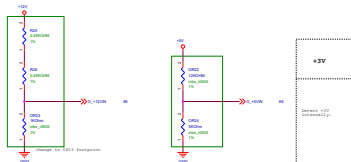
## PECI



## Hardware Monitor for Temperature



## Hardware Monitor for VIN



Standard Name

<b>ASUS</b>		Title : NCT6796D_BP-4	
ASUSTeK COMPUTER INC.		Engineer: Eagle	
Project Name	Project Name	Project Name	Project Name
Standard Circuit	Standard Circuit	Standard Circuit	Standard Circuit
Standard Circuit	Standard Circuit	Standard Circuit	Standard Circuit

Q\_CODE\_High byte

For Stealth mode

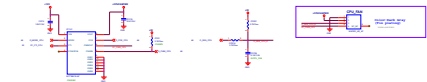
<Client Name>

<b>ASUS</b>		<b>Title :</b> NCT579ED-BF-S	
ASUSTeK COMPUTER INC.		Engineer: Eagle	
Rev	Project Name	Rev	
A3	Standard Circuit	Rev: 2/1/21	
Date: November 12, 2020	Drawn	By	Chk

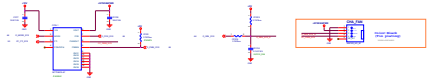


[W\_PUMP+] or [W\_PUMP-1]

Header	Max Current	Max Power	Default Speed	Shared Control
CPU FAN1	1A	12W	Q-Fan	A

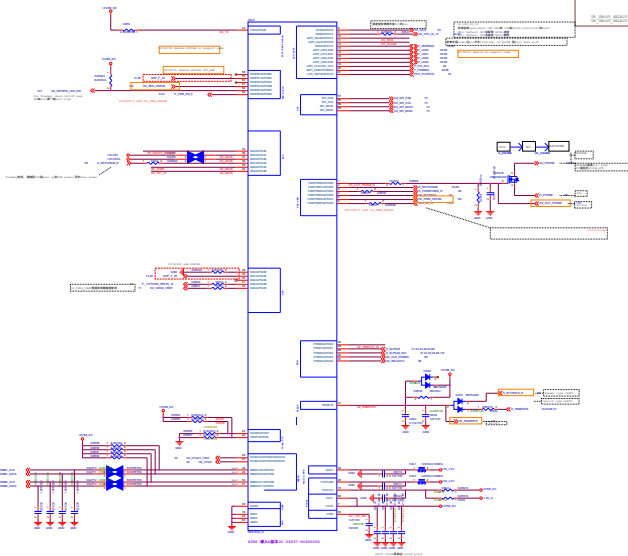
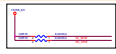


Header	Max Current	Max Power	Default Speed	Shared Control
CPU FAN2	1A	12W	Q-Fan	



Header	Max Current	Max Power	Default Speed	Shared Control
AIO PUMP	1A	12W	Full Speed	

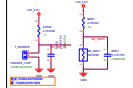




Only KB3728 Support

DIMM.2

Thermal Detect



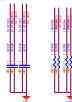
INTRUDER Test

Only KB3728 Support

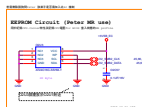
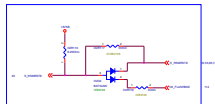
THERMALTRIP

Only KB3728 Support

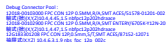
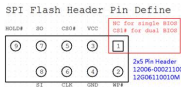
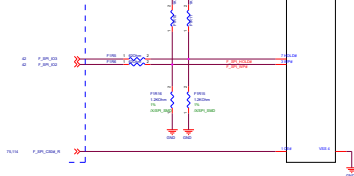
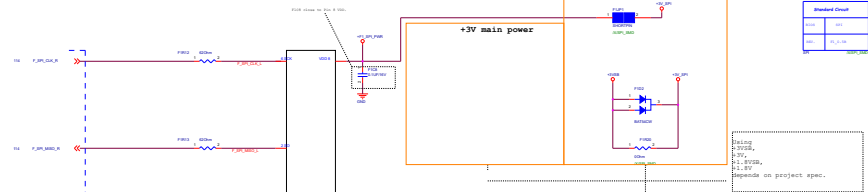
ADC CAP/Resistor



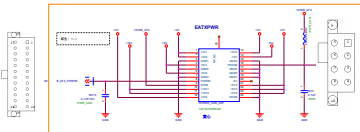








## 24 Pin ATX Connector

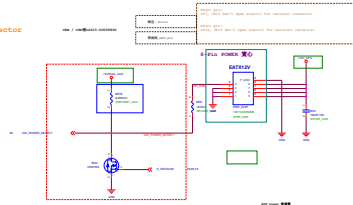


Bypass/EMI Capacitor

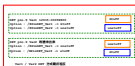


## 8 Pin +12V Connector

www.asus.com



www.asus.com



www.asus.com

www.asus.com

www.asus.com

www.asus.com



www.asus.com

www.asus.com

www.teknisi-indonesia.com

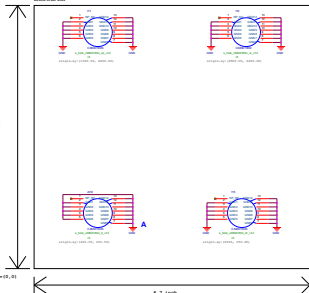
## Screw Hole

Fiducial Mask  
(光學點)

1.22

Define in the DMI

## Mini-ITX Screw Hole



6.6 Length

## Screw Select

	STANDARD (2.5 x 2.5)	MINI-ITX (2.5 x 2.5)
A	✓	✓
B	✓	✓
C	✓	✓
D	✓	✓
E	✓	✓
F	✓	✓
G	✓	✗
H	✓	✗

## M2 SCREW FOOTPRINT

A: 2.5 x 2.5



B: 2.5 x 2.5



C: 2.5 x 2.5



D: 2.5 x 2.5



大數光學點

小數光學點

大數十字光學點

小數十字光學點







OPTIONAL_1 (2x12)	OPTIONAL_2 (2x12)
OPTIONAL_3 (2x12)	OPTIONAL_4 (2x12)
OPTIONAL_5 (2x12)	OPTIONAL_6 (2x12)



OPTIONAL\_1 (2x12)

Rear Connector (Held)



180度connector

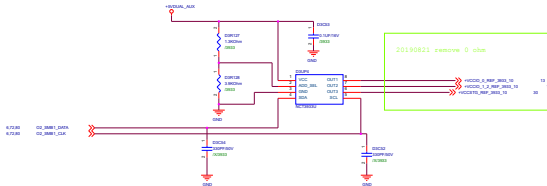


Rear Connector (Held)

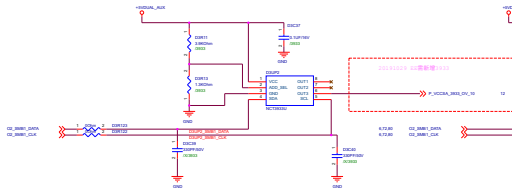


180度connector

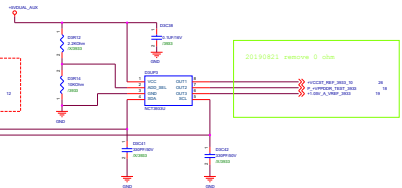




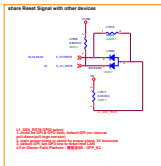
Address : 0x20



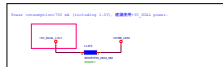
Address : 0x2A



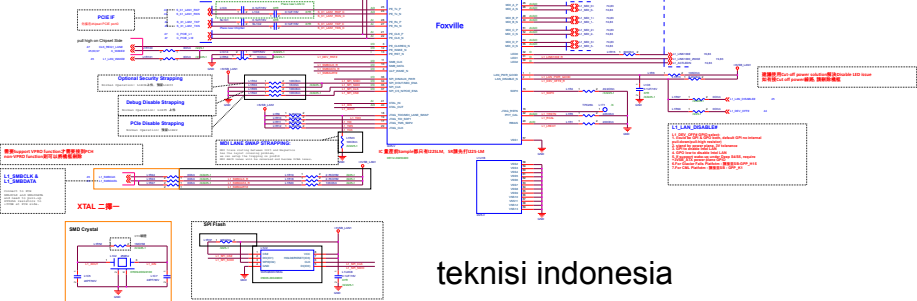




ROM location	use IEEE sample (MMS3.10)
IEEE External 1.0V	internal
IEEE External 1.0V	外部1.0V-1.0V(外部)



Standard Circuit	
NAME	DATE
SECTION	LAB #



使用ES0 sample 才需要外轉1.05V

1. 轉碼: i225 power monitor.pl.com=000 m5.
2. 轉碼: i225 power monitor.pl.com=最大. 建議使用 i225\_000.pl.com.

使用ES0 sample 才需要外轉1.05V

1.05V for I225, 500mA

Power Component place near each other!

20191030 Allen Remove

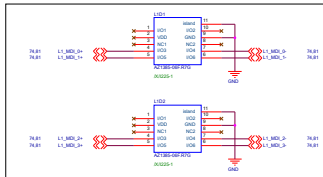
<Case Design>

		Title : I225_PWR	
ASUSTek Computer Inc.		Engineer: Tom Yang	
Size	Project Name		Rev
A2	Standard Circuit		0.00
Date	Thursday, December 12, 2019		Drawn A2 of 152

Delete it for EMS

STD標準

Delete it for EMS



Choose a proper LAN Connector in page Back I/O Connector

L1\_ACTLEDP  
L1\_ACTLEDN

GND

L1\_MD1\_3-  
L1\_MD1\_3+  
L1\_MD1\_2-  
L1\_MD1\_2+  
L1\_MD1\_1-  
L1\_MD1\_1+  
L1\_MD1\_0-  
L1\_MD1\_0+

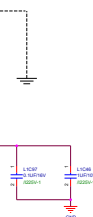
L1\_LINK1000#  
L1\_LINK100P

76

L1\_GTR



Place capacitors near the Lan Connector.  
Maybe need to be modified according to the different EMI consideration.



<Core Design>

		Title : L1_I225_Connector	
ASUSTek Computer Inc.		Engineer: Tom Yang	
Size	Project Name	Rev	
A3	Standard Circuit	0.00	



**Title :** CPTH (CNVi)

ASUSTek Computer Inc.

**Engineer:** Aaron\_Su

Size

C

Project Name

**Maximus XI Extreme**

Rev

R1.01

Date: Thursday, December 12, 2019

Sheet 84 of 152



**Title :** CPTH (CNVi)

ASUSTek Computer Inc.

**Engineer:** Aaron\_Su

Size

C

Project Name

**Maximus XI Extreme**

Rev

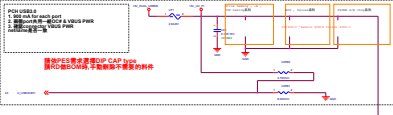
R1.01

Date: Thursday, December 12, 2019

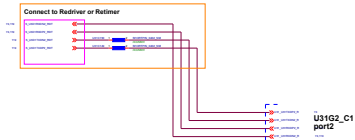
Sheet 85 of 152







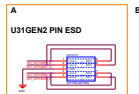
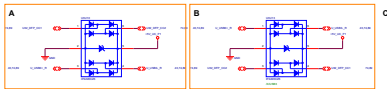
Connect to Connector

 U31G2\_C1 port1  
 U31G2\_C1 port2

 ASUS PIN ESD SPEC  
 Standby I/O: +7/-10KV  
 Front I/O: +7/-10KV

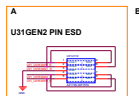
ESD 觸電防護方式:

觸電	觸電	A	B	C
Front I/O	Keep	Keep	Delete	Delete
Back I/O (Type 1) (Type 1)	Keep	Keep	Delete	Delete
Back I/O (Type 2) (Type 2)	Keep	Delete	Delete	Delete
Back I/O (Type 3) (Type 3)	Delete	Delete	Keep	Keep

Port 7,8



U31G2\_C1 port1



U31G2\_C1 port2

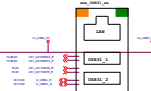


USB2.0 Guard  
 USB2.0 Guard

### USB2.0 Guard

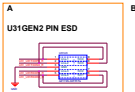
預防PCH USB2 Signal被Device寫入damaged問題

### Connect to Connector



### U31 GEN2 & GEN1 PIN ESD 橋接連導方式:

橋接	橋接	A	B
U31 GEN2 2 PIN ESD	Keep	Delete	Delete
U31 GEN1 1 PIN ESD	Delete	Delete	Keep

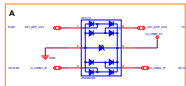


Port 3

### ESD橋接連導方式:

橋接	橋接	A	B	C
Front I/O	Keep	Keep	Delete	Delete
Back I/O Input (USB)	Keep	Keep	Delete	Delete
Back I/O Input (USB)	Keep	Delete	Delete	Delete
Back I/O Input (USB)	Delete	Delete	Keep	Keep

Port 3,4



ASUS

1. 使用板上的 USB2.0 GEN1 控制器  
2. 在板上的 USB2.0 GEN1 控制器上  
3. 連接 USB2.0 GEN1 控制器到 PWR  
4. 連接 USB2.0 GEN1 控制器到 PWR

請在 PCB 需求選擇 DIP CAP type  
請在 BOM 中，手動刪除不需要的料件

Connect to Chipset

Connect to Redriver or Retimer

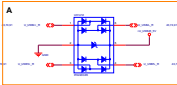
Connect to Redriver or Retimer

ASUS PIN ESD SPEC  
Back I/O : +/- 50V  
Front I/O : +/- 150V

ESD 接線選擇方式:

接線	A	B	C
Front I/O	Keep	Keep	Delete
Back I/O (Signal) 選擇	Keep	Keep	Delete
Back I/O (Signal) 選擇	Keep	Delete	Delete
Back I/O (Signal) 選擇	Delete	Delete	Keep

Port 5,6



Connect to Connector



Model: USB2.0 GEN1  
Model: USB2.0 GEN1

USB2.0 Guard

預防 PCH USB2 Signal 被 Device 高壓 Damage 問題

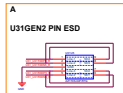
teknisi indonesia

USB5

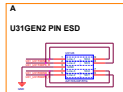
USB6

U31 GEN2 & GEN1 PIN ESD 接線選擇方式:

接線	A	B
U31 GEN2 & GEN1 PIN ESD	Keep	Delete
U31 GEN2 & GEN1 PIN ESD	Delete	Keep



Port 5



Port 6

ASUS

PCB USB2.0  
1. 確認PCB上是否有VBUS PWR  
2. 確認PCB上是否有VBUS PWR  
3. 確認connector VBUS PWR  
4. 確認PCB上是否有VBUS PWR

請於PES等式選擇UP CAP 1000  
請RD ROM時, 手動斷開不需要的材料

## Connect to Chipset

### Port 7



USB7

### Port 8



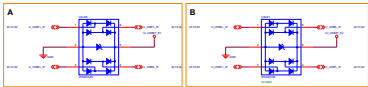
USB8

ASUS PIN ESD SPEC  
Back I/O +/- 8kV  
Front I/O +/- 15kV

ESD接線選擇方式:

接線	A	B	C
Power (G)	Keep	Keep	Delete
Back IO Input (GND)	Keep	Keep	Delete
Back IO Input (Data)	Keep	Delete	Delete
Back IO Input (Data)	Delete	Delete	Keep

Port 7, 8



## Connect to Connector



USB2.0 Guard

USB2.0 Guard

預防PCB USB2 Signal被Device高度damaged問題

PCB USB2.0  
1. 避免使用 BACK PIN  
2. 避免使用 USB 2.0 & USB PWR  
3. 避免使用 USB PWR  
4. 避免使用 USB PWR

請按PES等式選擇ZIP CAP 50V  
請RD接BOM時, 主動斷路不要誤的料件

## Connect to Chipset

### Port 9



### Port 10

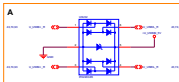


ASUS PIN ESD SPEC  
Back I/O: +/- 5KV  
Front I/O: +/- 10KV

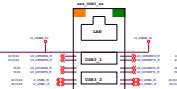
ESD 釋放選擇方式:

選擇	選擇	A	B	C
Front I/O	Keep	Keep	Delete	Delete
Back I/O (Keep) (選擇)	Keep	Keep	Delete	Delete
Back I/O (Keep) (選擇)	Keep	Delete	Delete	Delete
Back I/O (Keep) (選擇)	Delete	Delete	Keep	Keep

Port 9,10



## Connect to Connector



## USB2.0 Guard

預防PCH USB2.0 Signal被Device真塞damaged問題

ASUS

請依PES需求選擇DIP CAP type  
請RO 驗DCM時, 不能缺斷不重要的料件

Connect to Connector

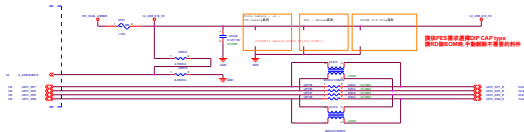
960.021-0001-00 960.021-0001-02 960.021-0001-03

USB2.0 Guard

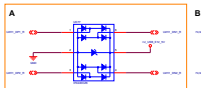
預防PCH USB2 Signal被Device 高壓damaged問題

Connect to Chipset

Front  
Port 11,12

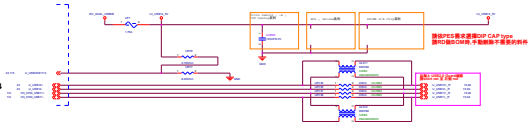


Port 11, 12



BACK

Port 13,14



Port 13,14



ASUS PIN ESD SPEC  
Back I/O : +/- 15KV  
Front I/O : +/- 10KV

ESD機電選擇方式:

機件	A	B	C
Front I/O	Keep	Keep	Delete
Back I/O Input/Output	Keep	Keep	Delete
Back I/O Input/Output	Keep	Delete	Delete
Back I/O Input/Output	Delete	Delete	Keep

Copyright © 2014

ASUS Title : 00P00100\_P000100

Version: 1.00

Keywords: ESD Protection

Standard Circuit

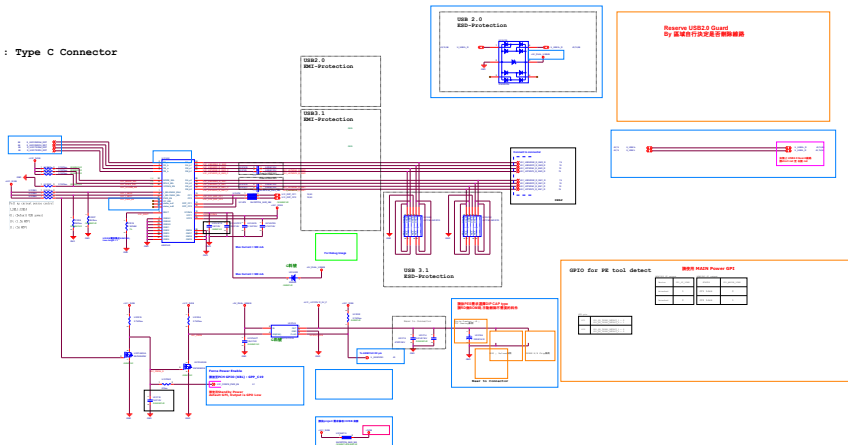
## Port B : Type A Connector

USB3.1  
ESD-Protection

USB2.0  
ESD-Protection

USB3.1/USB 2.0  
ESD-Protection

## Port A : Type C Connector

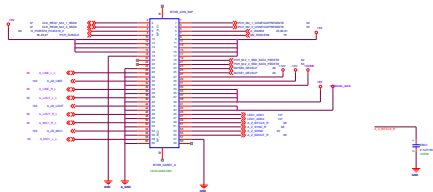
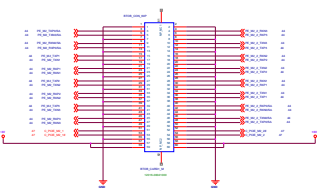


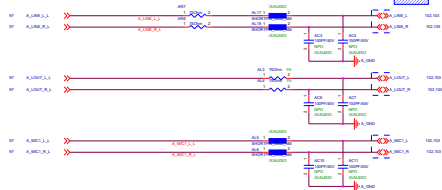


change to:  
 DT10 : 串接ROG logo  
 DT14 : AUI1088 1.0V/6.2V , 解VDDIO noise to

图1\*1.5mm间距焊孔

XX endriver在位板上, 所以audio card之连接





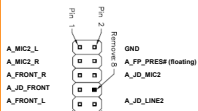
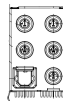
Close to  
connector

www.teknisi-indonesia.com



Standard Circuit	
ASUS	ASUS
SPDIF	A_2.17
ALC1220	ALC1220

## Front Panel

Back Panel  
7.1 Channel Connector(示意图)Back Panel  
5.1 Channel Connector  
+SPDIF OUT(Optical)(示意图)

## SPDIF OUT (Optical)(示意图)



&lt;Parent Name&gt;

<b>ASUS</b>		Title : ALC1220-2(Connector)	
Asus Computer Inc.		Engineer: Adam_Pan	
Model	Project Name	Standard Circuit	
A1			
Date	Version	Rev	Rev
2018/10/18	1.0	1.0	1.0



**Title :**      **ALC1220-3 (AMP)**

**ASUSTek Computer Inc.**

**Engineer:**                      **Adam\_Pan**

Size

**A3**

Project Name

**Standard Circiut**

Rev

**2.17**

Date:      **Thursday, December 12, 2019**

Sheet                      **100**                      of                      **152**

請依PES是否有上LDO 選擇相對應線路

二選一

自2390開始Audio Cap選擇如下  
ROG / Strix series : Nichicon  
PRIME / TUF : ELNA

Vendor strongly suggested for OVP ALC1220

\*Standard Name\*

<b>ASUS</b>		<b>Title :</b> ALC1220-8 (LDO)	
ASUSTek Computer Inc.		<b>Engineer:</b> Adam_Pan	
Part Name	Project Name	Rev	
A3	Standard Circuit	2.17	
Copyright © 2019		Page	107 of 108

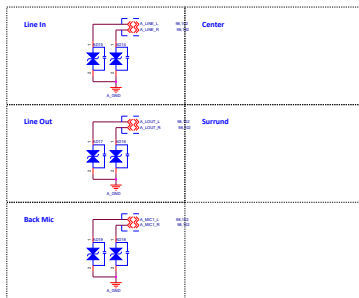


## VARISTOR

## Pin ESD spec (自Z370起spec)

Line Out	Headphone	Center	Surrund	Front Mic	Line In	Back Mic
5KV	5KV	4.5KV	4.5KV	5KV	4.5KV	5KV

For ALC1220 B2 : 所有Varistor皆需上件



Standard Name

<b>ASUS</b>		Title : ALC1220-4 (VARISTOR)	
ASUSTek Computer Inc.		Engineer: Adam_Pan	
Rev	Original Name	Standard Circuit	
A3		2.17	
Date: 2015/05/12		Page: 100 of 100	

# ASUS PCB Logo

PCB MADE IN CHINA



因應歐盟針對無線指令的修改,有Wi-Fi機種也請選用CE



無Wi-Fi機種請選用CE



2018年後FCC LOGO需使用新版本



Dxxxxx 文字在右方  
RoHS

文字在下方

Dxxxxx  
RoHS



CAN ICES-3 (B)/NMB-3(B)

## ASUS LOGO

X=1.5mm

X=2.5mm

X=3.0mm

X=3.5mm

X=4.0mm

X=4.5mm

X=5.0mm

X=6.0mm



X=2.0mm

X=5.5mm

M/B Default請用Symbol (2mm)和Symbol (5.5mm),若圖樣有包含Layout會通知從線路移除

©2018 ASUS

		Title : PCB Logo	
Asustek Computer Inc.		Engineer: Keli_Huang	
Drawn	Project Name	Silkscreen	
A3		0.2N	
Date: Thursday, December 13, 2018		2018 12 13 10:00	

# ASUS PCB Logo

## DRAM Slot Naming Rule

- DIMM slot "" 命名方式, 若 MR team 建議先採
1. DIMM\_x1 就叫做 DIMM\_A1\_STAR, DIMM\_B1\_STAR ... 以此類推
  2. DIMM\_x2 就叫做 DIMM\_A2\_STAR, DIMM\_B2\_STAR ... 以此類推
  3. RD請與MR確認後提Modify給Layout確認""擺放位置



## 烏克蘭LOGO



## Model name字體選擇



## 新版KCC LOGO (2018-8-6之後開案新單1.00的機種使用)

無Wi-Fi Module機種  
R-R-MSQ-XXXXXXX00000000

有Wi-Fi Module機種  
R-R-MSQ-XXXXXXX00000000

WiFi IC on board特殊機種  
R-C-MSQ-XXXXXXX00000000



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P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
80	V	V	temp_M01_00010
P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
82	V	V	temp_T_2014013
P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
80	X	V	temp_T_2014014
P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
82	X	V	temp_T_2014015
P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
80	X	X	temp_T_2014016
P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
82	X	X	temp_T_2014017
P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
X	V	X	temp_T_2014018
P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
80	V	X	temp_T_2014019
P13	DATA	BIT	狀態
100' 00' 00"	10' 00' 00"	10' 00' 00"	
82	V	X	temp_T_2014020

<Default Name>

		Title : M2_TEXT	
ASUSTEK COMPUTER INC.		Engineer: Grace Wu	
Size	Project Name		Rev
A3	Silkacreen		0.01
Date	Thursday, December 13, 2016	Scale	100% off 100%



- LED Driver對LED內部的Pin
- LED Driver對連接外部的Pin
- 根據IO規格可更換其他功能的Pin即
- 依據Intel/AMD平台標記Power pin
- 依據IO規格/空間，標記LED組數/驅動/Header
- 註解

#### Addressable Header (支援2組)

第1組

ADD LED Power1

Addressable LED Header 1

#### ADD\_HEADER1 反白文字區

(請依主機板板型選擇對應的文字區)

ROG/ ROG STRIX



Channel /TUF Gaming



#### ADD\_HEADER2 反白文字區

(請依主機板板型選擇對應的文字區)

ROG/ ROG STRIX



Channel /TUF Gaming



Channel Number

ASUS		Title : ADD_Header	
Engineer: Kaitzer_Luo			
Date	Project Name		
Version	LED Standard Circuit		
		Created	



**Title :** **LGA1200 (XDP)**

ASUSTek Computer Inc.

**Engineer:** **Martino\_Yang**

Size

**A2**

Project Name

**Maximus XII Extreme**

Rev

**R1.00**

Date: **Thursday, December 12, 2019**

Sheet **38** of **126**





**Title :**        **Node**

ASUSTek Computer Inc.

**Engineer:**        **Aaron\_Su**

Size

Project Name

Rev

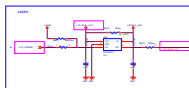
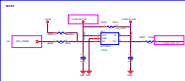
C

**Maximus XII Extreme**

R1.01

Date:        Thursday, December 12, 2019

Sheet        110        of        152




20190731 Remove GF17 CPU\_OV

CPU\_OV Default GPI  
High: VCCIN --->2.7V  
Low: VCCIN ---->3.04V

Z97\_R1.01

<Variant Name>

		Title : CPU_OV	
ASUSTek Computer Inc.		Engineer: Eason	
Size A	Project Name Z270-STRIX		Rev 1.02
Date: Thursday, December 12, 2019		Sheet 112 of 152	

Follow SIO to select +3V or +3V\_S00X



Modify Part Number by color

2 第1

For Intel S0ix



For not Intel S0ix

SOM	TPM Header	Onboard TPM
N/A	mount	mount
/X	unmount	unmount
/TPM HEADER	mount	unmount
/TPM IC	unmount	mount

\*Omitted Section

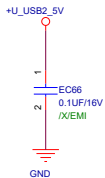
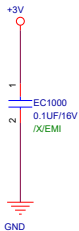
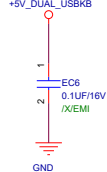
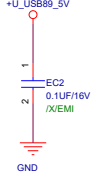
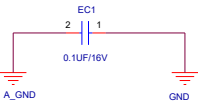
		Title : TPM	
ASUSTeK Computer INC		Engineer: Ben Hsieh	
Rev	Project Name	File	
A1	Standard Circuit	4.2	
Date: Thursday, December 10, 2020		Page	112 of 120











Title		
<Title>		
Size	Document Number	Rev
A	Z390 Golden board	R1.01
Date:	Monday, December 23, 2019	Sheet 117 of 152

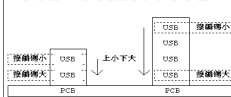
# PL CAP



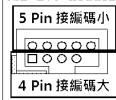
# PL CAP



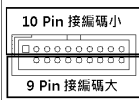
## USB Connector



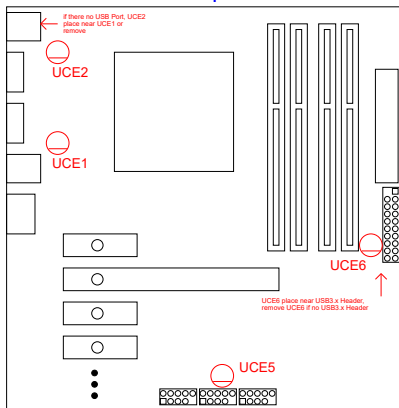
## USB 2.0 Header



## USB 3.0 Header



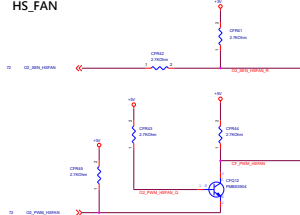
## USB Power CAP recommend placement

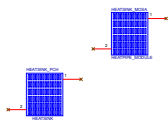


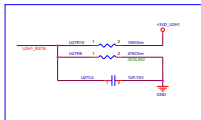
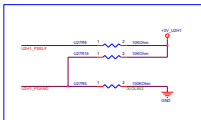
©2009 ASUS



# HS\_FAN



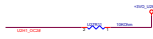




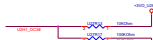
1. 選擇 USB 連接埠，選擇 USB 連接埠
2. 選擇 USB 連接埠，選擇 USB 連接埠
3. 選擇 USB 連接埠，選擇 USB 連接埠



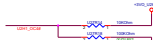
BOM select	USB 連接埠	接 On-board Device	接使用 Downstream Port
U27R7	mount	unmount	unmount
U27R15	unmount	unmount	mount



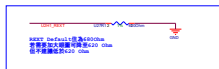
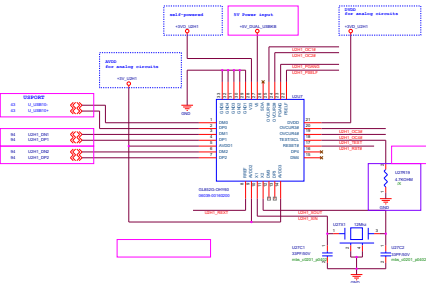
BOM select	USB 連接埠	接 On-board Device	接使用 Downstream Port
U27R11	mount	unmount	unmount
U27R16	unmount	unmount	mount



BOM select	USB 連接埠	接 On-board Device	接使用 Downstream Port
U27R13	mount	unmount	unmount
U27R17	unmount	unmount	mount



BOM select	USB 連接埠	接 On-board Device	接使用 Downstream Port
U27R14	mount	unmount	unmount
U27R18	unmount	unmount	mount



USB2C27 (10A1P6.3V) 和 USB2C27B (10A1P6.3V) 的輸出電壓為 4.8V，但不建議低於 4.2V。GND 也不建議低於 4.2V。GND


© 2018 ASUS

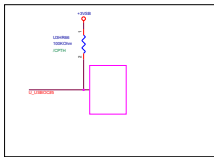
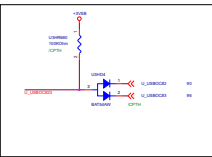
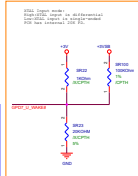
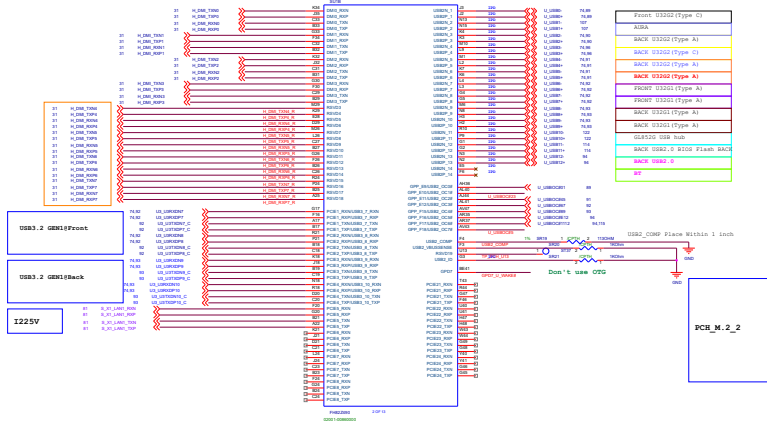


# For DOA/FA improvement

NET	TestPoint name	Note
H_SKTOCC#	AT3	
S_RTCRST#	AT4	
S_SRTCST#	AT5	
S_INTRUDER#	AT6	
O_CASEOPEN#	AT88	

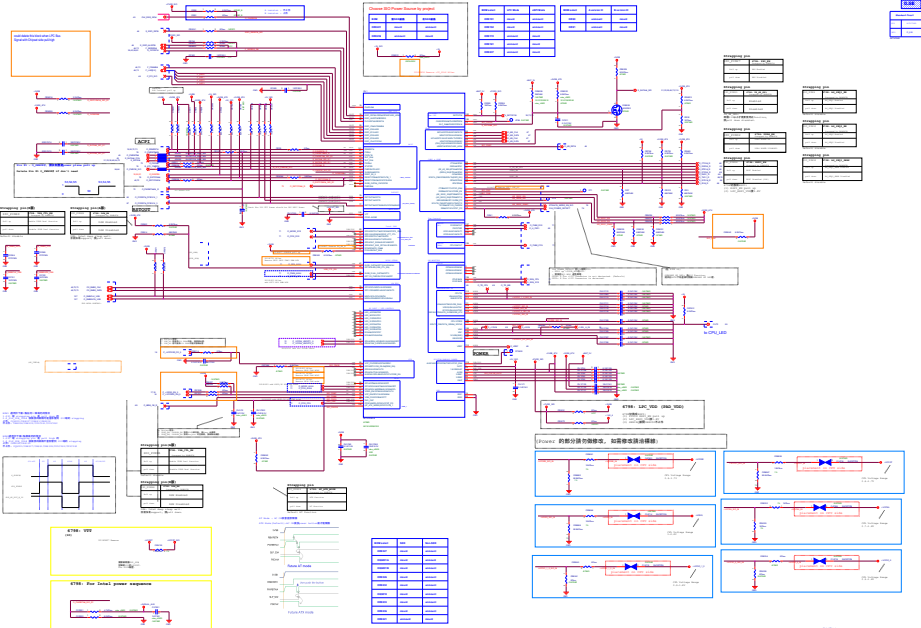
<Variant Name>

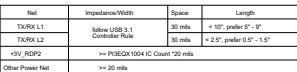
		<b>Title :</b> DOA/FA improvement	
ASUSTEK COMPUTER INC		<b>Engineer:</b> Aaron Su	
Size A	Project Name <b>Maximus XI Extreme</b>		Rev R1.01
Date: Thursday, December 12, 2019	Sheet	151	of 152



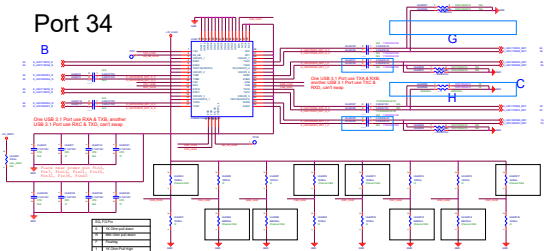


<div> <div>0.58</div> <div>Standard 5: Overall</div> </div>	
<div> <div>0.58</div> <div>0.58</div> </div>	<div> <div>0.58</div> <div>0.58</div> </div>
<div> <div>0.58</div> <div>0.58</div> </div>	<div> <div>0.58</div> <div>0.58</div> </div>





Delete the Re-Order (it is not needed by Project)  
 Modify Input Signal 1 to TDRX Signal Name by Project  
 Modify Output Signal 1 to TDRX Signal Name by Project  
 Choose PIGE0104 from Power Signal by PIGE0104 code  
 If I/F TDRX output signal sends to AM1543A, U04H33CA & U04H35C change  
 to U04H33CA, U04H35C & U04H36C by Project  
 If I/F TDRX output signal sends to U04H33CA, U04H35C & U04H36C change  
 to U04H33CA, U04H35C & U04H36C by Project  
 If I/F TDRX output signal sends to U04H33CA, U04H35C & U04H36C change  
 to U04H33CA, U04H35C & U04H36C by Project  
 If I/F TDRX output signal sends to AM1543A, U04H33CA & U04H35C change  
 to AM1543A, U04H33CA & U04H35C by Project  
 If I/F TDRX output signal sends to U04H33CA, U04H35C & U04H36C change  
 to U04H33CA, U04H35C & U04H36C by Project  
 If I/F TDRX output signal sends to AM1543A, U04H33CA & U04H35C change  
 to AM1543A, U04H33CA & U04H35C by Project  
 If I/F TDRX output signal sends to U04H33CA, U04H35C & U04H36C change  
 to U04H33CA, U04H35C & U04H36C by Project  
 If I/F TDRX output signal sends to AM1543A, U04H33CA & U04H35C change  
 to AM1543A, U04H33CA & U04H35C by Project  
 If I/F TDRX output signal sends to U04H33CA, U04H35C & U04H36C change  
 to U04H33CA, U04H35C & U04H36C by Project

[illegible][illegible]

